EXPRESS MAIL NO. EL990358589US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Daniel B. Penney Attorney Docket No.: 500987.02
Filed : Concurrently herewith
Title : PREDECODE COLUMN ARCHITECTURE AND METHOD

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

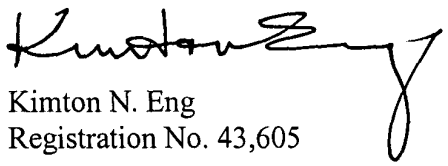
Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior Application No. 10/014,013, filed November 5, 2001. The references listed on the attached Form PTO-1449 were submitted to and/or cited by the Patent and Trademark Office in this prior application and, therefore, are not required to be provided in this application. If the Examiner wishes, copies will be provided upon request. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP



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Enclosure:
Form PTO-1449

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FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500987.02	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Daniel B. Penney	
		FILING DATE Concurrently herewith	GROUP ART UNIT Not Yet Assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,021,688	06/04/91	Leforestier et al.	307	463	
	AB	5,592,434	01/07/97	Iwamoto et al.	365	233	
	AC	5,781,497	07/14/98	Patel et al.	365	230.06	
	AD	5,825,714	10/20/98	Kohno	365	230.06	
	AE	5,881,017	03/09/99	Matsumoto et al.	365	230.04	
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AK							
	AL							
	AM							
	AN							
	AO							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AP	Choi, Y. et al., "16-Mb Synchronous DRAM with 125-Mbyte/s Data Rate", IEEE Journal of Solid-State Circuits, Vol. 29, No. 4, April 1994, pp. 529-533.
	AQ	Sunaga, T. et al., "A Full Bit Prefetch Architecture for Synchronous DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995, pp. 998-1005.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).